independent memory circuits shared by both the first and processor and the second processor for receiving the successive sets of input data and providing the successive sets of output data,

the method comprising, for a set of input data and a set of output data, the following steps:

a configuration step in which the memory system is set up by means of control commands associated with the set of input data and the set of output data; and

an execution step in which, on the basis of the control commands, the memory system:

ensures that input data and output data are not simultaneously required for writing and reading from one of the plurality of independent memory circuits.

REMARKS

Claims 1-5 remain pending in this application. Claims 1, 4 and 5, the independent claims, have been amended. Favorable reconsideration is respectfully requested.

In the Office Action, Claims 1-5 were rejected under 35 U.S.C. ∋ 102 as being anticipated by U.S. Patent 4,734,850 (Torii et al.)

Applicant respectfully submits that the rejected claims as amended are patentable for at least the following reasons.

Claim 1 as amended is directed to a data processing arrangement including a

first processor for providing successive sets of input data, a second processor for receiving successive sets of output data and a memory system including a plurality of independent memory circuits shared by the first processor and the second processor for receiving the successive sets of input data and providing the successive sets of output data. The arrangement also includes a master controller for setting up the plurality of independent memory circuits of said memory system using control commands associated with a set of input data and a set of output data and a control unit for, on the basis of the control commands, ensuring that input data and output data are not simultaneously required for writing and reading from one of the plurality of independent memory circuits.

As understood by Applicant, Torii et al. relates to a data process system that includes plural storage means each capable of concurrent and intermediate reading and writing of a set of data signals.

Nothing has been found in Torii et al., however that teaches a control unit for, on the basis of the control commands, ensuring that input data and output data are not simultaneously required for writing and reading from one of the plurality of independent memory circuits, as recited in Claim 1.

At least for this reason, Claim 1 is believed patentable over Torii et al.

Independent Claims 4 and 5 recite similar features as recited in Claim 1, and are believed allowable for at least the same reason.

A review of the other art of record has failed to reveal anything which, in Applicant's opinion, would remedy the deficiencies of the art discussed above, as reference a against the independent claims. Those claims are therefore believed patentable over the art of record.

The other rejected claims in this application are each dependent from one or another of the independent claims discussed above and are therefore believed patentable for the same reasons. In addition, however, each dependent claim is also deemed to define an additional aspect of the invention, and should be individually considered on its own merits.

In view of the foregoing amendments and remarks, Applicant respectfully requests favorable reconsideration and early passage to issue of the present application.

Applicant's undersigned attorney may be reached by telephone at the number given below.

Respectfully submitted,

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CERTIFICATE OF MAILING

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On May 18, 2002

By _____
Rick de Pinho, Reg. 41,703

Appendix of Marked-up Claims

1. A data processing arrangement comprising:

a first processor for providing successive sets of input data;

a second processor for receiving successive sets of output data;

a memory system comprising a plurality of independent memory circuits shared by the first processor and the second processor for receiving the successive sets of input data and providing the successive sets of output data;

a master controller for setting up the plurality of independent memory circuits of said memory system using control commands associated with a set of input data and a set of output data; and

a control unit for, on the basis of the control commands, ~~selecting a first memory circuit and generating a write-address for the first memory circuit when a data from the set of input data is provided by the first processor, and for, on the basis of the control commands, selecting a second memory circuit and generating a read-address for the second memory circuit when a data from the set of output data is required by the second processor~~ ensuring that input data and output data are not simultaneously required for writing and reading from one of the plurality of independent memory circuits.

4. (As Amended) A memory system comprising:

a plurality of independent memory circuits for receiving successive sets of input data and for providing successive sets of output data;

a control unit being programmable by means of control commands associated with a

set of input data and a set of output data and, on the basis of these control commands, for ~~selecting a first memory circuit and generating a write-address for the first memory circuit, when a data from the set of input data is received, and for selecting a second memory circuit and generating a read-address for the second memory circuit, when a data from the set of output data is provided~~ ensuring that input data and output data are not simultaneously required for writing and reading from one of the plurality of independent memory circuits.

5. (As Amended) A method of processing data in a data processing arrangement including a first processor for providing successive sets of input data, a second processor for receiving successive sets of output data and a memory system including a plurality of independent memory circuits shared by both the first and processor and the second processor for receiving the successive sets of input data and providing the successive sets of output data,

the method comprising, for a set of input data and a set of output data, the following steps:

a configuration step in which the memory system is set up by means of control commands associated with the set of input data and the set of output data; and

an execution step in which, on the basis of the control commands, the memory system:

~~selects a first memory circuit and generates a write-address for the first memory circuit for a data belonging to the set of input data;~~

~~selects a second memory circuit and generates a read-address for the second~~

~~memory circuit for a data belonging to the set of output data~~

ensures that input data and output data are not simultaneously required for writing and reading from one of the plurality of independent memory circuits.